WHAT IS CLAIMED IS:

1. A circuit for modifying output data of storage means, the storage means outputting a data word with a width of 2^N (where N is a natural number) bytes, the data word being stored at respective addresses, starting at an address specified as a multiple of 2^N by an address signal, on the storage means, the circuit comprising:

a data register for retaining correction data with the width of 2^N bytes thereon;

an address register for retaining a correction address thereon;

a correspondence detector, which receives the address signal and the correction address and determines whether or not correspondence is found between the correction address and one of a number 2^N of addresses starting at, or preceding, the address specified by the address signal; and

a stored data selecting section for selectively outputting, on a byte-by-byte basis, either the output data of the storage means or the correction data in accordance with the address signal and the correction address if the correspondence detector has found the correspondence,

wherein the circuit delivers the output of the stored data selecting section as modified stored data.

2. The circuit of Claim 1, wherein the stored data se-

lecting section comprises:

a byte selector for selectively outputting, on a byte-by-byte basis, either the output data of the storage means or the correction data; and

a byte selection controller for controlling the selective output of the byte selector in accordance with an N^{th}-bit value of the address signal, a low-order-$(N+1)$-bit value of the correction address and the output of the correspondence detector.

3. The circuit of Claim 2, wherein the byte selection controller controls the byte selector in such a manner that an M^{th} byte (where M is an integer and $0 \leqq M < 2^N$) of the correction data is selected as an M^{th}-byte output of the byte selector if

a) the correspondence detector has found the correspondence; and

b)-i) the N^{th}-bit value of the address signal is equal to an N^{th}-bit value of the correction address and a low-order-N-bit value of the correction address is less than $(M+1)$; or

b)-ii) the N^{th}-bit value of the address signal is different from the N^{th}-bit value of the correction address and the low-order-N-bit value of the correction address is equal to or greater than $(M+1)$,

and that an M^{th}-byte output of the storage means is selected as the M^{th}-byte output of the byte selector if the conditions a) and b) are not met.

4. The circuit of Claim 1, further comprising a data rotator for rotating the correction data on a byte-by-byte basis by the number of bytes that corresponds to a low-order-N-bit value of the correction address,

wherein the stored data selecting section receives the output of the data rotator instead of the correction data.

5. The circuit of Claim 1, wherein if a result obtained by subtracting a value of the correction address excluding low-order N bits thereof from a value of the address signal excluding low-order N bits thereof is "0" or "1", then the correspondence detector finds the correspondence.

6. A circuit for modifying output data of storage means, the storage means outputting a data word with a width of 2^N (where N is a natural number) bytes, the data word being stored at respective addresses, starting at an address specified as a multiple of 2^N by an address signal, on the storage means, the circuit comprising:

a number of data registers, each said data register retaining correction data with the width of 2^N bytes thereon;

the same number of address registers, each said address register retaining a correction address thereon, the data and address registers forming the same number of register pairs;

the same number of correspondence detectors, each said correspondence detector being associated with one of the register pairs and determining, responsive to the address signal and the correction address retained on the associated address register, whether or not correspondence is found between the correction address and one of a number 2^N of addresses starting at the address specified by the address signal or between the correction address and one of a number $(2^N - 1)$ of addresses preceding the address specified by the address signal;

a data register selector, which receives the outputs of the correspondence detectors and outputs, as selected correction data, the correction data retained on one of the data registers that is associated with one of the correspondence detectors that has found the correspondence;

an address register selector, which also receives the outputs of the correspondence detectors and outputs, as a selected correction address, the correction address retained on one of the address registers that is associated with the correspondence detector that has found the correspondence; and

a stored data selecting section for selectively outputting, on a byte-by-byte basis, either the output data of the

storage means or the selected correction data, output from the data register selector, in accordance with the address signal and the selected correction address, output from the address register selector, if the correspondence detector has found the correspondence,

wherein the circuit delivers the output of the stored data selecting section as modified stored data.

7. The circuit of Claim 6, wherein the stored data selecting section comprises:

a byte selector for selectively outputting, on a byte-by-byte basis, either the output data received from the storage means or the selected correction data received from the data register selector; and

a byte selection controller for controlling the selective output of the byte selector in accordance with an N^{th}-bit value of the address signal, a low-order-$(N+1)$-bit value of the selected correction address output from the address register selector and the outputs of the correspondence detectors.

8. The circuit of Claim 7, wherein the byte selection controller controls the byte selector in such a manner that an M^{th} byte (where M is an integer and $0 \leqq M < 2^N$) of the correction data is selected as an M^{th}-byte output of the byte selector if

a) one of the correspondence detectors has found the correspondence; and

b)-i) the N^{th}-bit value of the address signal is equal to an N^{th}-bit value of the selected correction address and a low-order-N-bit value of the selected correction address is less than (M+1); or

b)-ii) the N^{th}-bit value of the address signal is different from the N^{th}-bit value of the selected correction address and the low-order-N-bit value of the selected correction address is equal to or greater than (M+1),

and that an M^{th}-byte output of the storage means is selected as the M^{th}-byte output of the byte selector if the conditions a) and b) are not met.

9. The circuit of Claim 6, further comprising a data rotator for rotating the selected correction data on a byte-by-byte basis by the number of bytes that corresponds to a low-order-N-bit value of the selected correction address,

wherein the stored data selecting section receives the output of the data rotator instead of the selected correction data.

10. The circuit of Claim 6, wherein if a result obtained by subtracting a value of the correction address excluding low-order N bits thereof from a value of the address signal

excluding low-order N bits thereof is "0" or

if the result is "1" but a low-order-N-bit value of the correction address is not "0", then

each said correspondence detector finds the correspondence.